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EXAMINER	
HUISMAN, DAVID J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 12/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/721,152	SISKA, CHARLES P.	
	Examin r	Art Unit	
	David J. Huisman	2183	

-- The MAILING DATE of this communication appears on th cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9-11,13-21 and 32-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed..

6)☒ Claim(s) *1-7,9-11,13-21 and 32-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 November 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-7, 9-11, 13-21, and 32-34 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Request for RCE and Amendment as received on 9/17/2004.

Specification

3. The title of the invention that appears in the amendment filed on 9/17/2004 ("Method For Decoding Composite VLIW Packets Utilizing A Tree Structure") does not match the amended title from the amendment filed on 4/16/04 ("Method For Decoding Composite VLIW Packets"). A new title is required that is clearly indicative of the invention to which the claims are directed. Please amend the old title to realize the new title.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-7, 9-11, 13-21, and 32-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hull et al., U.S. Patent No. 5,922,065 (as applied in the previous Office Action

and herein referred to as Hull) in view of Gupta et al., U.S. Patent No. 6,457,173 (as applied in the previous Office Action and herein referred to as Gupta).

6. Referring to claim 1, Hull has taught a method for decoding a first composite packet in a processor, said method comprising the steps of:

a) providing assembly code for each one of a plurality of instructions in a first combination of instructions in said first composite packet. It is inherent that assembly code is provided for packet instructions because assembly code is basic code that an assembler operates upon in order to translate the assembly code into machine code (0s and 1s), which are the only values "understood" by the processor.

b) matching a template in said first composite packet to a known template corresponding to one of a plurality of known syntaxes. See Fig.3 of Hull and note that each packet comprises a template. When a packet is fetched, the template will be matched against all of the possible templates shown in Fig.4. These templates then correspond to known syntaxes, which include information about the types of instructions in the packet and how they are executed. For instance, template 0 corresponds to the MII syntax, i.e., a packet that includes a type of memory instruction and two integer or immediate instructions. Hull has not taught that the plurality of known syntaxes are arranged as a plurality of first level nodes in a tree structure, wherein each of a plurality of second level nodes in said tree structure includes a combination of instruction types, and wherein each of a plurality of third level nodes in said tree structure includes an instruction type. However, Gupta has taught such a concept. See Fig.2, components 134 and 136, and column 12, lines 1-3. These first level nodes represent the instruction syntaxes (template). Second level nodes 138, 140, and 142, represent a combination of instruction types.

For instance, node 140 represents a combination of instructions including a compare (CMPP) instruction, a logical AND (LAND) instruction, and an integer add (IADD) instruction. Finally, Gupta has taught that third level nodes such as 144 and 146 represent an instruction type. For instance, node 146 shows a type of instruction that has a predicate field (pr), a first source being a general purpose register (gpr), a second source being either a general purpose register or a short literal (gpr s), and a destination being a general purpose register (gpr). Gupta has further disclosed that this system may simplify the decoding logic. See column 21, lines 8-14. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Hull such that Hull includes the tree structure taught by Gupta.

c) a plurality of paths extends between node levels and wherein each node of said plurality of first level nodes and said plurality of second level nodes has a path to a node of a different node level. See Fig.2, and note the plurality of paths between levels. Also, each node in the first level will have a path to a second level, and each node in the second level will have a path to the third level. Applicant should realize that Gupta's Fig.2 is just showing an example of paths for certain nodes. The figure would not be large enough to show all paths, connections, and nodes within the tree. However, it should be realized that each valid first level node (template) would have a path to the second level, because valid templates represent specific bundles of instructions (see column 12, lines 20-38, and note that each template defines instructions that may issue concurrently, and the second level specifies those instructions). For instance, looking at Fig.4 of Hull, if a first first-level node corresponded to template 1, then a path would connect that node to a second level node representing instruction combinations that would satisfy the M-I-I slot requirements. Furthermore, if a second first-level node corresponded to template 4, then a path

would connect that node to a second level node representing instruction combinations that would satisfy the M-M-I slot requirements, and so on. In addition, the instructions at the second level can clearly have different formats, which are represented in level 3. Clearly, all instructions must have a corresponding format, and therefore, there will be paths from second level nodes to third level nodes. Without these paths, the placements of the destination and source operands within the instruction, along with a predicate and opcode, would not be known. Consequently, these paths must exist.

d) matching said one of said plurality of known syntaxes with a resolved packet syntax. From Fig.4, once the template is matched, a resolved packet syntax of the instruction will be determined, i.e., if the template of a packet corresponds to template 0, then the resolved packet index would be a specific type of M-unit instruction, a first I-unit instruction, and a second I-unit instruction. Hull has not taught matching using the tree structure, but as described above, it would have been obvious to include the tree structure of Gupta in the system of Hull, and therefore, since the syntaxes are in the tree of Gupta, the matching of syntaxes would occur using the tree structure.

e) using said resolved packet syntax to determine assembly code associated with execution of said first combination of instructions. If the packet has a template with a value of 0, then assembly code corresponding to the M-unit instruction will be determined, assembly code corresponding to the first I-unit instruction will be determined, and assembly code for the second I-unit instruction will be determined.

f) providing assembly code associated with execution of said first combination of instructions. It is inherent that the assembly code will be executed.

7. Referring to claim 2, Hull in view of Gupta has taught a method as described in claim 1. Hull has further taught that said step of matching said one of said plurality of known syntaxes comprises the step of matching each term in said one of said plurality of known syntaxes against a respective term in said resolved packet syntax. For a packet that is assigned a template value of 6, for instance, slot 0 must contain a memory instruction (M-unit), slot 1 must contain a floating-point instruction (F-unit), and slot 2 must contain an integer or immediate instruction (I-unit). Since the processor knows that the first instruction of the packet is a memory instruction, it will find a matching memory type instruction and send it to slot 0. It will then find a matching instruction for slot 1, and so on.

8. Referring to claim 3, Hull in view of Gupta has taught a method as described in claim 2. Hull has further taught that said step of matching said one of said plurality of known syntaxes is a direct matching step. It is inherent that the matching step is direct because one item is matched against another term, then these terms are being directly matched.

9. Referring to claim 4, Hull in view of Gupta has taught a method as described in claim 1. Hull has further taught that said assembly code associated with execution of said first combination of instructions specifies an issue group for said first combination of instructions. See column 3, line 66, to column 4, line 19. Also, see Fig.4 and note that for template 0, the three sub-instructions form an issue group (referred to as an instruction group in Hull) in that they are contiguous instructions that may be executed concurrently.

10. Referring to claim 5, Hull in view of Gupta has taught a method as described in claim 1. Hull has further taught that said assembly code associated with execution of said first combination of instructions specifies a plurality of issue groups for said first combination of

instructions. See column 4, lines 43-60. Also, see Fig.4 and note that for template 1, the double lines separating the slot 2 instruction from the slot 1 instruction indicate that the slot 2 instruction is part of a different issue group that that of the slot 0 and slot 1 instructions.

11. Referring to claim 6, Hull in view of Gupta has taught a method as described in claim 1. Hull has further taught that said assembly code associated with execution of said first combination of instructions identifies a chained instruction in said first combination of instructions, wherein said chained instruction belongs to an issue group in a second composite packet. See Fig.4, template 1, and column 4, lines 43-67. It should be realized that for template 1, the slot 0 and slot 1 instructions make up at least part of a first instruction group, and the slot 2 instruction is part of a second instruction group which would include instructions from a subsequent packet (if the stop bit is 0).

12. Referring to claim 7, Hull in view of Gupta has taught a method as described in claim 1. Hull has further taught that said assembly code associated with execution of said first combination of instructions identifies a plurality of chained instructions in said first combination of instructions, wherein said plurality of chained instructions belong to respective issue groups in a second composite packet. See Fig.4, template 5, and column 4, lines 43-67. It should be realized that for template 5, the slot 0 instruction makes up at least part of a first instruction group, and the slot 1 and slot 2 instructions are part of a second instruction group, which could include instructions from a subsequent packet (if the stop bit is 0).

13. Referring to claim 9, Hull in view of Gupta has taught a method as described in claim 1. Hull has further taught that said known template identifies at least one issue group in said first composite packet. See Fig.4, and note that template 0 specifies an issue group that includes all

three of the instructions within the packet. Template 1, on the other hand, specifies that the slot 0 and slot 1 instructions are part of a first instruction group and the slot 2 instruction is part of a second instruction group.

14. Referring to claim 10, Hull in view of Gupta has taught a method as described in claim 1. Hull has further taught that said known template identifies a chained instruction in said first combination of instructions, wherein said chained instruction belongs to an issue group in a second composite packet. See Fig.4, template 1, and note that the chained slot 2 instruction would be part of a second instruction group (if the stop bit = 0 for that particular VLIW packet), where the first instruction group comprises at least the slot 0 and slot 1 instructions.

15. Referring to claim 11, Hull in view of Gupta has taught a method as described in claim 1. Hull has further taught that said known template identifies a plurality of chained instructions in said first combination of instructions, wherein said plurality of chained instructions belong to respective issue groups in a second composite packet. See Fig.4, template 5, and note that the chained slot 1 and slot 2 instructions would be part of a second instruction group (if the stop bit = 0 for that particular VLIW packet), where the first instruction group comprises at least the slot 0 instruction.

16. Referring to claim 13, Hull in view of Gupta has taught a method as described in claim 1. Hull has further taught that said composite packet in said processor consists of 128 bits. See Fig.3.

17. Referring to claim 14, Hull in view of Gupta has taught a method as described in claim 1. Hull has not explicitly taught that said composite packet in said processor consists of 256 bits. However, it should be noted that changes in size and/or range, absent evidence of unexpected

results from the change in size and/or change, are generally not given patentable weight or would have been obvious improvements. See In re Rose, 105 USPQ 237 (CCPA 1955). Hull has explicitly taught that a packet is 128 bits but he has further taught that the packet can be any N-bit field. See column 5, lines 59-65. A person of ordinary skill in the art would have recognized that a larger VLIW packet size would allow for larger data (i.e. larger constants and memory addresses), more templates, and more overall instructions, which would result in increase parallelism. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have the composite packet in said processor consist of 256 bits.

18. Referring to claim 15, Hull in view of Gupta has taught a method as described in claim 1. Hull has not explicitly taught that each instruction in said first combination of instructions consists of 16 bits. However, it should be noted that changes in size and/or range, absent evidence of unexpected results from the change in size and/or change, are generally not given patentable weight or would have been obvious improvements. See In re Rose, 105 USPQ 237 (CCPA 1955). Hull has explicitly taught that each instruction in a VLIW packet is 41 bits. See Fig.3 and column 3, lines 52-55. A person of ordinary skill in the art would have recognized that these instructions could be made smaller in order to reduce the size of the overall program (smaller instructions take up less memory resources than larger instructions). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have each instruction consist of 16 bits.

19. Referring to claim 16, Hull in view of Gupta has taught a method as described in claim 1. Hull has not explicitly taught that each instruction in said first combination of instructions consists of 32 bits. However, it should be noted that changes in size and/or range, absent

evidence of unexpected results from the change in size and/or change, are generally not given patentable weight or would have been obvious improvements. See In re Rose, 105 USPQ 237 (CCPA 1955). Hull has explicitly taught that each instruction in a VLIW packet is 41 bits. See Fig.3 and column 3, lines 52-55. A person of ordinary skill in the art would have recognized that these instructions could be made smaller in order to reduce the size of the overall program (smaller instructions take up less memory resources than larger instructions). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have each instruction consist of 32 bits.

20. Referring to claim 17, Hull in view of Gupta has taught a method as described in claim 1. Hull has further taught that each instruction in said first combination of instructions consists of 41 bits. See Fig.3 and column 3, lines 52-55.

21. Referring to claim 18, Hull in view of Gupta has taught a method as described in claim 1. Hull has further taught that said first combination of instructions comprises at least two instructions. See Fig.3 and Fig.4 and note that the VLIW packet format and template allow for as many as three individual instructions to be combined.

22. Referring to claim 19, Hull in view of Gupta has taught a method as described in claim 1. Hull has further taught that said first combination of instructions comprises at least one issue group. See Fig.4 and note that template 0 specifies that all three instructions are part of the same issue group while template 1 specifies that the slot 0 and slot 1 instructions are part of a first issue group and the slot 2 instruction is part of a second issue group.

23. Referring to claim 20, Hull in view of Gupta has taught a method as described in claim 24. Hull has further taught that said at least one issue group comprises at least one instruction. See column 4, lines 4-7.

24. Referring to claim 21, Hull in view of Gupta has taught a method as described in claim 1. Hull has further taught that said template bits consist of at least five bits. See Fig.3 and note that four bits are used to specify a "template" which maps each slot to the appropriate functional unit and specifies instruction group boundaries. In addition, bit 0 of the VLIW packet is for a stop bit, which determines whether an instruction group ends after the last instruction in the bundle (i.e. after the slot 2 instruction). Since all of these bits play a part in controlling how and when the instructions in the VLIW are executed, they can all be considered part of the template. Therefore, the overall template would be 5 bits.

25. Referring to claim 32, Hull in view of Gupta has taught a method as described in claim 1. Hull has further taught that said instruction type is selected from a group consisting of instruction type A, instruction type I, instruction type M, instruction type F, instruction type B, and instruction type LX. See Fig.2 of Hull.

26. Referring to claim 33, Hull in view of Gupta has taught a method as described in claim 2. Hull has further taught that said matching said one of said plurality of known syntaxes is an indirect matching step. The "American Heritage® Dictionary of the English Language defines "indirect" as "not proceeding straight to the point or object" and "secondary". It should be realized that the packet will only match one of the syntaxes shown in the first level of nodes in Gupta's tree (Fig.2, components 134 and 136). If the packet is compared to a first syntax and a match does not occur, then the packet will have to be compared to subsequent syntaxes until the

match is found. This is an indirect matching step since the match did not occur in the first comparison (straight to the point). Instead, it happened after a subsequent syntax was matched (secondary).

27. Referring to claim 34, Hull in view of Gupta has taught a method as described in claim 2. Gupta has further taught that said step of matching said one of said plurality of known syntaxes matches each said term at one of said plurality of first level nodes in said tree structure. See the first level of Gupta's tree in Fig.2 (components 134 and 136). It should be noted that the instruction starts off at root 132 and then the instruction template is determined by matching each term to the respective term in the template, where the template is shown in Fig.4 of Hull. For instance, if the VLIW instruction in Hull corresponds to template 1 (M I || I) as shown in Fig.4, then when performing the matching step in Gupta's tree, it will first be compared to template 0 (component 134). However, template 0 would possibly be set to be the same as template 0 of Hull (M I I), and therefore, a match would not occur because (M I I) does not match (M I || I). Consequently, the system will try and match the instruction with template 1, where a match will be successful if template 1 of Gupta is the same as template 1 of Hull.

Response to Arguments

28. Applicant's arguments filed on April 13, 2004, have been fully considered but they are not persuasive.

29. In the remarks, Applicant argues the novelty/rejection of claim 1 on page 11 of the remarks, in substance that:

> "Figure 2 of Gupta illustrates the structure of an if-tree. Column 12, lines 1-3, of Gupta simply state that the overall structure of the if-tree defines how each instruction is built. Figure 2 of Gupta illustrates "OR" nodes (oval-shaped) and 'AND" nodes (boxed-shaped). Furthermore, Gupta

states that "the OR nodes denote a selection between the children of the node such that only one choice (one branch) extends to the next level. Stated another way, each level of the tree is either a conjunction (AND) or disjunction (OR) of the sub-trees at the lower level." Gupta, column 12, lines 7-13. Furthermore, in Figure 2 of Gupta, there are nodes that do not have paths to other node levels (i.e. there are dead ends),"

30. This arguments are not found persuasive for the following reasons:

a) The examiner has addressed this argument in the rejection of claim 1(c) above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (571) 272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJH
David J. Huisman
December 9, 2004

RICHARD L. ELLIS
PRIMARY EXAMINER